Patent
Attorney's Docket No. 032219-007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Earl McCune and Wendell Sander for HIGH-EFFICIENCY AMPLIFIER OUTPUT LEVEL AND BURST CONTROL.

Also enclosed are:

[X] 3 sheet(s) of [ ] formal [X] informal drawing(s);

[ ] a claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 is [ ] hereby made to _____ filed in _____ on _____; [ ] in the declaration;

[ ] a certified copy of the priority document;

[ ] a Constructive Petition for Extensions of Time;

[ ] _____ statement(s) claiming small entity status;

[ ] an Assignment document;

[ ] an Information Disclosure Statement; and

[X] Other: a postcard.

The declaration of the inventor(s) [X] also is enclosed [ ] will follow.

[ ] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§119 and/or 365 to _____ filed in _____ on _____; the entire content of which is hereby incorporated by reference.--

The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		**EXTRA CLAIMS**	**RATE**	**FEE**
Basic Application Fee					$760.00
Total Claims	11	MINUS 20 =	0	x $18.00	0
Independent Claims	2	MINUS 3 =	0	x $78.00	0
If multiple dependent claims are presented, add $260.00					0
Total Application Fee					760.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					0
Add Assignment Recording Fee of $40.00 if Assignment document is enclosed					0
TOTAL APPLICATION FEE DUE [FEE NOT INCLUDED]					**$760.00**

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Respectfully submitted,

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Date: February 8, 1999

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HIGH-EFFICIENCY AMPLIFIER OUTPUT LEVEL AND BURST CONTROL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to amplifier output level control.

2. State of the Art

Battery life is a significant concern in wireless communications devices such as cellular telephones, pagers, wireless modems, etc. Radio-frequency transmission, especially, consumes considerable power. A contributing factor to such power consumption is inefficient power amplifier operation. A typical RF power amplifier for wireless communications operates with only about 10% efficiency. Clearly, a low-cost technique for significantly boosting amplifier efficiency would satisfy an acute need.

Furthermore, most modern digital wireless communications devices operate on a packet basis. That is, the transmitted information is sent in a series of one or more short bursts, where the transmitter is active only during the burst times and inactive at all other times. It is therefore also desirable that control of burst activation and deactivation be controlled in an energy-efficient manner, further contributing to extended battery life.

Power amplifiers are classified into different groups: Class A, Class B, Class AB, etc. The different classes of power amplifiers usually signify different biasing conditions. In designing an RF power amplifier, there is usually a trade-off between linearity and efficiency. The different classes of amplifier operation offer designers ways to balance these two parameters.

Generally speaking, power amplifiers are divided into two different categories, linear and non-linear. Linear amplifiers (e.g. Class A amplifiers and Class B push-pull amplifiers), maintain high linearity, resulting in faithful reproduction of the input signal at their output since the output signal is linearly proportional to the input signal. In non-linear amplifiers (e.g. single-ended Class B, and Class C

amplifiers), the output signal is not directly proportional to the input signal. The resulting amplitude distortion on the output signal makes these amplifiers most applicable to signals without any amplitude modulation, which are also known as constant-envelope signals.

Amplifier output efficiency is defined as the ratio between the RF output power and the input (DC) power. A major source of power amplifier inefficiency is power dissipated in the transistor. A Class A amplifier is inefficient since current flows continuously through the device. Conventionally, efficiency is improved by trading-off linearity for increased efficiency. In Class B amplifiers, for example, biasing conditions are chosen such that the output signal is cut off during half of the cycle unless the opposing half is provided by a second transistor (push-pull). As a result, the waveform will be less linear. The output waveform may still be made sinusoidal using a tank circuit or other filter to filter out higher and lower frequency components.

Class C amplifiers conduct during less than 50% of the cycle, in order to further increase efficiency; i.e., if the output current conduction angle is less than 180 degrees, the amplifier is referred to as Class C. This mode of operation can have a greater efficiency than Class A or Class B, but it typically creates more distortion than Class A or Class B amplifiers. In the case of a Class C amplifier, there is still some change in output amplitude when the input amplitude is varied. This is because the Class C amplifier operates as a controlled current source--albeit one that is only on briefly--and not a switch.

The remaining classes of amplifiers vigorously attack the problem of power dissipation within the transistor, using the transistor merely as a switch. The underlying principle of this amplifier is that a switch ideally dissipates no power, for there is either zero voltage across it or zero current through it. Since the switch's V-I product is therefore always zero, there is no dissipation in this device. A Class E power amplifier uses a single transistor, in contrast with a Class D

power amplifier, which uses two transistors

In real life, however, switches are not ideal. (Switches have turn on/off time and on-resistance.) The associated dissipation degrades efficiency. The prior art has therefore sought for ways to modify so-called "switch-mode" amplifiers (in which the transistor is driven to act as a switch at the operating frequency to minimize the power dissipated while the transistor is conducting current) so that the switch voltage is zero for a non-zero interval of time about the instant of switching, thereby decreasing power dissipation. The Class E amplifier uses a reactive output network that provides enough degrees of freedom to shape the switch voltage to have both zero value and zero slope at switch turn-on, thus reducing switching losses. Class F amplifiers are still a further class of switch-mode amplifiers. Class F amplifiers generate a more square output waveform as compared to the usual sinewave. This "squaring-up" of the output waveform is achieved by encouraging the generation of odd-order harmonics (i.e., x3, x5, x7, etc.) and suppressing the even-order harmonics (i.e., x2, x4, etc.) in the output network.

An example of a known power amplifier for use in a cellular telephone is shown in Figure 1. GSM cellular telephones, for example, must be capable of programming output power over a 30dBm range. In addition, the transmitter turn-on and turn-off profiles must be accurately controlled to prevent spurious emissions. Power is controlled directly by the DSP (digital signal processor) of the cellular telephone, via a DAC (digital to analog converter). In the circuit of Figure 1, a signal GCTL drives the gate of an external AGC amplifier that controls the RF level to the power amplifier. A portion of the output is fed back, via a directional coupler, for closed-loop operation. The amplifier in Figure 1 is not a switch-mode amplifier. Rather, the amplifier is at best a Class AB amplifier driven into saturation, and hence demonstrates relatively poor efficiency.

Survey of Prior Patents

Control of the output power from an amplifier is consistently shown as requiring a feedback structure, as exemplified in U.S. Patents 4,392,245; 4,992,753; 5,095,542; 5,193,223; 5,369,789; 5,410,272; 5,697,072 and 5,697074. Other references, such as U.S. Patent 5,276,912, teach the control of amplifier output power by changing the amplifier load circuit. U.S. Patent 4,994,757 teaches that the power supply voltage can be varied to improve the efficiency of power amplifiers, but that further control of the actual amplifier output signal magnitude requires automatic control through a feedback process. U.S. Patent 5,126,688 addresses the control of linear amplifiers using feedback control to set the actual amplifier output power combined with periodic adjustment of the power amplifier operating voltage to improve the operating efficiency of the power amplifier. U.S. Patent 5,604,924 teaches a simplified control system for an analog cellular telephone. The operating voltage of a power amplifier operated in Class C is fed back and used to adjust the output power through operation of a variable voltage circuit implemented as a switch-mode DC-DC converter.

Despite the teachings of the foregoing references, a number of problems remain to be solved, including the following: simple control of amplifier output power, without the need for feedback or circuit configuration changes; allowing the amplifier to support bursted operation, such as in a time-division multiple access (TDMA) system; maintenance of high efficiency amplifier performance during power control changes, and high efficiency of DC to RF conversion from the original power supply through the amplifier, even during TDMA bursted operation; and elimination of incidental amplitude modulation of the power amplifier from ripple noise on the output of the switch-mode DC-DC converter.

SUMMARY OF THE INVENTION

The present invention, generally speaking, provides for high-efficiency power control of a high-efficiency (e.g., hard-limiting or switch-mode) power

amplifier. In one embodiment, the invention exploits the recognition that, for a constant-resistance circuit, power is equal to the square of the voltage across the circuit divided by the resistance of the circuit. In the case of certain switch mode amplifiers, such as Class E and Class F amplifiers, as well as saturated linear amplifiers, the amplifier may reasonably be regarded as having a constant resistance with varying power supply. In an exemplary embodiment, the supply voltage is controlled using a combination of two stages, a switch-mode converter stage that accomplishes gross power level control and a subsequent linear regulator stage that accomplishes more precise power envelope control, e.g., burst control. Control circuitry for the amplifier is simplified by combining control signals for power amplifier ramp-up transition, power level during a TDMA burst, and ramp-down transition, into a single control signal, and by eliminating feedback control (which also eliminates errors in the feedback control of output power due to the use of detecting diodes). Output noise from the variable output switch-mode voltage converter stage is filtered using the linear regulator stage that accomplishes burst control, further increasing circuit efficiency. Energy efficiency during ramp-up to the desired output power, during the burst at all output power levels, and during ramp-down from the transmitted power, is maximized. Reasonable expected efficiencies for the switch-mode converter stage and the linear regulator stage are 90% and 80%, respectively. A high-efficiency switch-mode amplifier may have an efficiency on the order of 80%, enabling an overall efficiency of greater than 50% to be achieved, comparing very favorably with current efficiencies of about 10%.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a block diagram of a known power amplifier with output power controlled by varying the power supply voltage;

Figure 2 is a plot comparing saturated Class AB power amplifier output power versus operating voltage with the mathematical model $V = \sqrt{PR}$;

Figure 3 is a block diagram of a power amplifier in accordance with an exemplary embodiment of the present invention;

Figure 4 is a waveform diagram illustrating operation of one embodiment of the invention; and

Figure 5 is a waveform diagram illustrating operation of another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figure 3, a block diagram is shown of a power amplifier in accordance with an exemplary embodiment of the present invention. A switch-mode (or saturated) nonlinear amplifier has applied to it a voltage produced by a power control stage. In an exemplary embodiment, the voltage V applied to the nonlinear amplifier is controlled substantially in accordance with the equation

$$V = \sqrt{PR}$$

where P is the desired power output level of the amplifier and R is the resistance of the amplifier. In the case of a switch-mode or saturated amplifier, the resistance R may be regarded as constant. The power control stage receives a DC input voltage, e.g., from a battery, and receives a power level control signal and outputs a voltage in accordance with the foregoing equation.

The efficacy of directly controlling output power of nonlinear amplifiers over a wide dynamic range by solely varying the operating voltage is demonstrated by Figure 2, showing a plot comparing saturated Class AB power amplifier output power versus operating voltage with the mathematical model $V = \sqrt{PR}$.

Referring now to Figure 3, a power control circuit in accordance with an exemplary embodiment of the invention is shown. A power control stage includes a switch-mode converter stage and a linear regulator stage connected in series. The switch-mode converter may be a Class D device, for example, or a switch-mode power supply (SMPS). The switch-mode converter efficiently steps down the DC

voltage to a voltage that somewhat exceeds but that approximates the desired power-amplifier operating voltage level. That is, the switch-mode converter performs an efficient gross power level control. The switch-mode converter may or may not provide sufficiently fine control to define ramp portions of a desired power envelope.

The linear regulator performs a filtering function on the output of the switch-mode converter. That is, the linear regulator controls precise power-envelope modulation during a TDMA burst, for example. The linear regulator may or may not provide level control capabilities like those of the switch-mode converter.

Note that, depending on the speed of the switch-mode converter and the linear regulator, the power control stage may be used to perform power control and/or amplitude modulation. A control signal PL/BURST is input to a control block, which outputs appropriate analog or digital control signals for the switch-mode converter and the linear regulator. The control block may be realized as a ROM (read-only memory) and/or a DAC (digital to analog converter).

Referring to Figure 4, a waveform diagram is shown, illustrating operation of one embodiment of the invention. The waveforms A and B represent analog control signals applied to the switch-mode converter and to the linear regulator, respectively. The waveforms V_1 and V_2 represent the output voltages of the switch-mode converter and to the linear regulator, respectively. Assume that the switch-mode converter has a relatively large time constant, i.e., that it ramps relatively slowly. When the control signal A is set to a first non-zero power level, the voltage V_1 will then begin to ramp toward a commensurate voltage. Because of the switch-mode nature of the converter, the voltage V_1 may have a considerable amount of ripple. An amount of time required to reach that voltage defines the wakeup period. When that voltage is reached, the control signal B is raised and lowered to define a series of transmission bursts. When the control signal B is raised, the voltage V_2 ramps quickly up to a commensurate voltage, and when the

control signal B is lowered, the voltage V_2 ramps quickly down. Following a series of bursts (in this example), the control signal A is raised in order to increase the RF power level of subsequent bursts. The control signal B remains low during a wait time. When the voltage V_1 has reached the specified level, the control signal B is then raised and lowered to define a further series of transmission bursts.

The voltage V_2 is shown in dotted lines superimposed on the voltage V_1. Note that the voltage V_2 is less than the voltage V_1 by a small amount, greater than the negative peak ripple on the voltage V_1. This small difference between the input voltage of the linear regulator V_1 and the output voltage of the linear regulator V_2 makes overall high-efficiency operation possible.

Referring to Figure 5, in accordance with a different embodiment of the invention, the switch-mode converter is assumed to have a relatively short time constant; i.e., it ramps relatively quickly. Hence, when the control signal A is raised, the voltage V_1 ramps quickly to the commensurate voltage. The control signal B is then raised, and the voltage V_2 is ramped. The time difference between when the control signal A is raised on the control signal B is raised defines the wake up time, which may be very short, maximizing sleep time and power savings. The control signal B is then lowered at the conclusion of the transmission burst, after which the control signal A is lowered. Following the example of Figure 4, in Figure 5, when the control signal A is next raised, it defines a higher power level. Again, the voltage V_2 is superimposed in dotted lines on the voltage V_1.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

What is claimed is:

1. A variable output RF power amplifier comprising:

voltage regulator means for producing a specified voltage within a range of voltages in accordance with a control signal; and

a power amplifier having the specified voltage as a supply voltage.

2. The apparatus of Claim 1, wherein the voltage regulator means comprises a first switch-mode converter stage and a second linear regulator stage.

3. The apparatus of Claim 2, wherein the switch-mode converter stage provides coarse level control and the linear regulator stage provides fine ramp control.

4. The apparatus of Claim 3, wherein the power amplifier is hard-limited.

5. The apparatus of Claim 4, wherein the power amplifier is a saturated amplifier selected from the group of Class A and Class AB amplifiers.

6. The apparatus of Claim 3, wherein the power amplifier is a switch-mode amplifier.

7. The apparatus of Claim 3, wherein the power amplifier is a Class C amplifier.

8. The apparatus of Claim 2, wherein the switch-mode converter stage provides level control and ramp control.

9. The apparatus of Claim 2, wherein the linear regulator stage provides ramp control and level control.

10. The apparatus of Claim 2, further comprising means for receiving said control signal and in response thereto producing a first control signal for the switch-mode converter stage and a second control signal for the linear regulator stage.

11. A method of controlling a power level of a power amplifier, comprising:

generating a specified voltage in accordance with a control signal; and

applying the specified voltage to a power amplifier as a supply voltage of the switch-mode power amplifier.

ABSTRACT OF THE DISCLOSURE

The present invention, generally speaking, provides for high-efficiency power control of a high-efficiency (e.g., hard-limiting or switch-mode) power amplifier. In one embodiment, the invention exploits the recognition that, for a constant-resistance circuit, power is equal to the square of the voltage across the circuit divided by the resistance of the circuit. In the case of certain switch mode amplifiers, such as Class E and Class F amplifiers, as well as saturated linear amplifiers, the amplifier may reasonably be regarded as having a constant resistance with varying power supply. In an exemplary embodiment, the supply voltage is controlled using a combination of two stages, a switch-mode converter stage that accomplishes gross power level control and a subsequent linear regulator stage that accomplishes more precise power envelope control, e.g., burst control. Control circuitry for the amplifier is simplified by combining control signals for power amplifier ramp-up transition, power level during a TDMA burst, and ramp-down transition, into a single control signal, and by eliminating feedback control (which also eliminates errors in the feedback control of output power due to the use of detecting diodes). Output noise from the variable output switch-mode voltage converter stage is filtered using the linear regulator stage that accomplishes burst control, further increasing circuit efficiency. Energy efficiency during ramp-up to the desired output power, during the burst at all output power levels, and during ramp-down from the transmitted power, is maximized. Reasonable expected efficiencies for the switch-mode converter stage and the linear regulator stage are 90% and 80%, respectively. A high-efficiency switch-mode amplifier may have an efficiency on the order of 80%, enabling an overall efficiency of greater than 50% to be achieved, comparing very favorably with current efficiencies of about 10%.

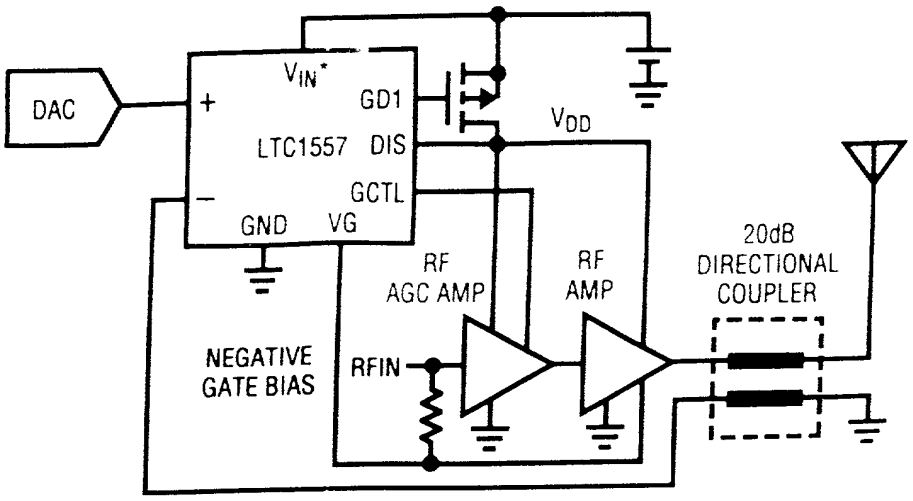


FIG 1 (PRIOR ART)

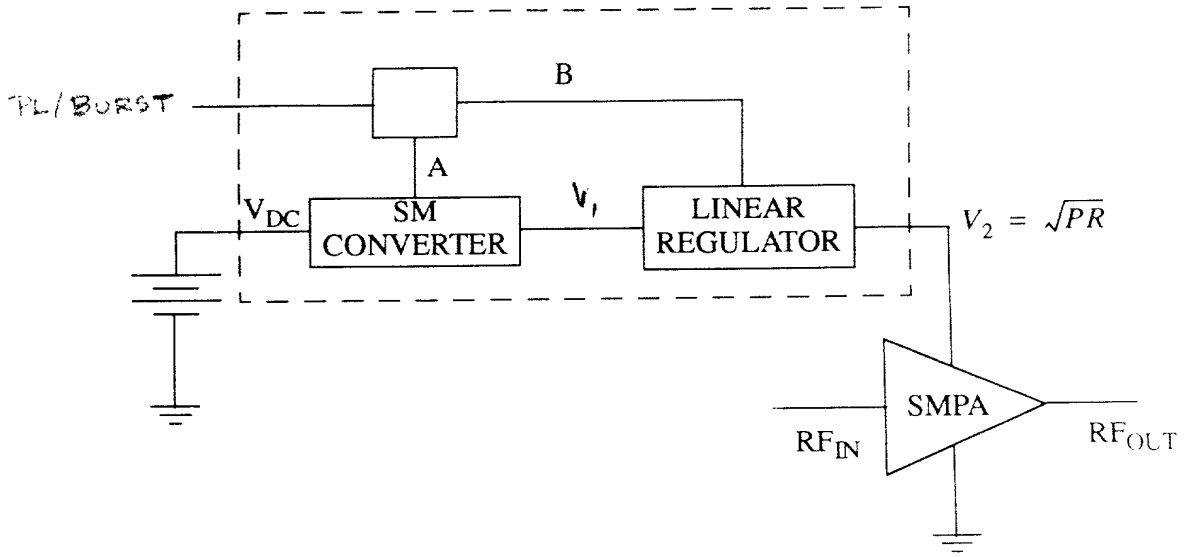


FIG 3

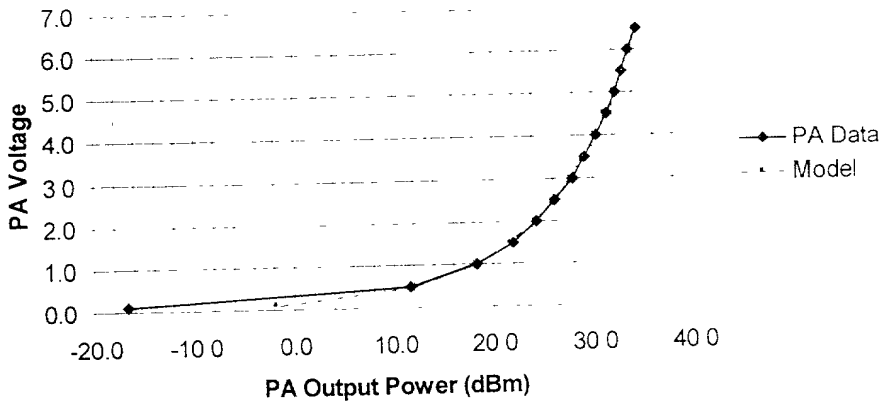
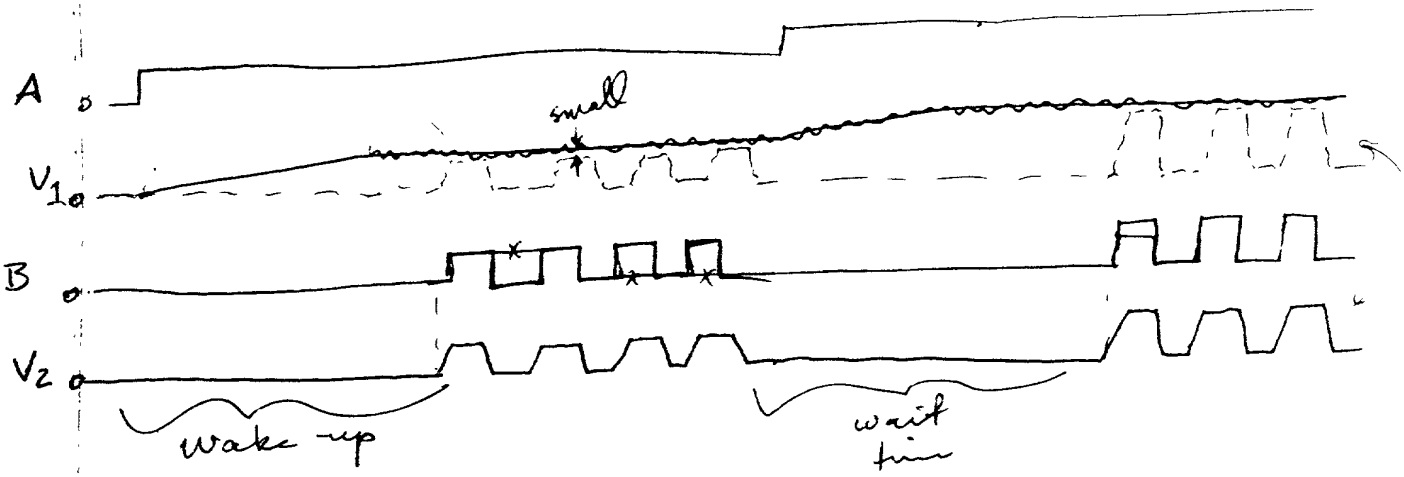

7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
PA Voltage
-20.0
-10.0
0.0
10.0
20.0
30.0
40.0
PA Output Power (dBm)
PA Data
Model

FIG 2

FIG 4



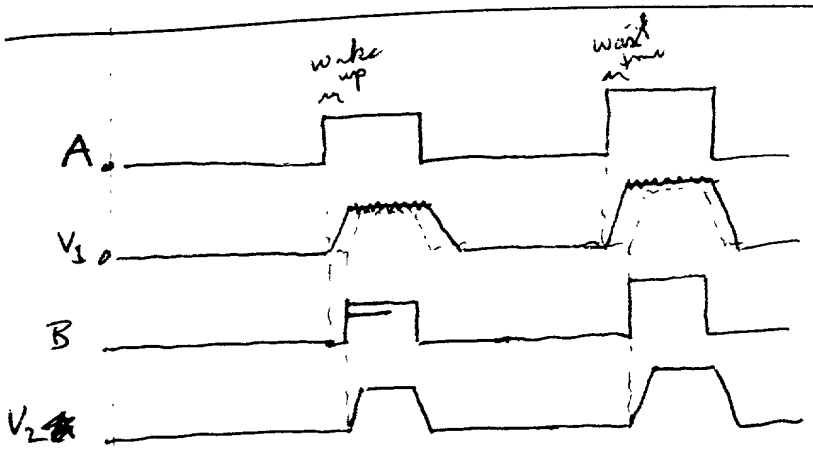


FIG 5

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032219-007

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

HIGH-EFFICIENCY AMPLIFIER OUTPUT LEVEL AND BURST CONTROL

the specification of which

(check one) ☒ is attached hereto;

☐ was filed on _____ as

Application No. _____

and was amended on _____; (if applicable)

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No. 032219-007

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(01/99)